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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,300	07/25/2003	Jeong Ho Park	OF03P107/US	1904

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,300	PARK, JEONG HO	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003 through 09 Feb 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract **not exceed 150 words** in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The examiner suggests changing "comprising" to "including" (in line 2) and shortening the abstract by highlighting the inventive aspect(s) of the current invention.

2. The disclosure is objected to because of the following informalities:

On page 6, in lines 4-18, it seems that reference characters "50" and "60" should be interchanged because Fig. 1B shows layer "50" being formed under layer "60", i.e., note the description in lines 8-9 on page 6 of the specification.

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

At claim 1, line 10, the examiner suggests deleting "the" before "first spacers", since this is the first recitation of "first spacers";

at claim 1, line 24, the examiner suggests deleting "the" before "second spacers", since this is the first recitation of "second spacers"; and

at claim 1, line 25, "patter" should read "pattern".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woerlee et al. (6,406,963 B2; hereinafter, "**Woerlee**") in view of **Wu** (5,856,226).

Regarding claim 1:

Woerlee discloses a method of forming short-channel transistors, the method comprising the steps of:

forming a first oxide layer 7 and a sacrificial layer 10 one after another on a semiconductor substrate 1 and etching the sacrificial layer, thus forming a residual sacrificial layer pattern 10 (Fig. 1 and Col. 5, lines 31-35);

conducting an ion implantation using the residual sacrificial layer pattern 10 as a mask, thus forming an LDD ion-implant layer 11 in the semiconductor substrate (Fig. 1 and Col. 5, lines 54-55);

forming first spacers 13 on both side walls of the sacrificial layer pattern 10 (Fig. 2);

conducting an ion implantation using the residual sacrificial layer pattern 10 and the first spacers as a mask, thus forming a source/drain ion-implant layer 14/15 under the LDD ion-implant layer 11 (Figs. 1-2);

forming a nitride layer 17 and a second oxide layer 18 one after another on the whole surface of the former resultant object (NOTE: annealing must be performed after ion-implant layers 14/15 are formed in order to activate the dopants, therefore, this limitation is not considered to carry patentable weight);

conducting CMP process to the extent that an upper surface of the residual sacrificial layer pattern 10 is exposed (Fig. 4 and Col. 6, lines 26-32), and removing the residual sacrificial layer pattern 10 through etching (Fig. 6 and Col. 6, lines 34-52);

conducting an ion implantation 22 on the substrate, thus forming a punch-stop ion implant layer 20 (Fig. 6);

etching the first oxide layer 7 under the portion where the residual sacrificial layer pattern 10 is removed, and forming a gate insulating layer 24 (Figs. 6-7; Col. 6, lines 42-43; and Col. 7, lines 25-26); and

forming a gate 21 on the portion where the residual sacrificial layer pattern is removed (Fig. 11 and Col. 8, lines 34-35).

Woerlee **lacks** forming second spacers on side walls of a portion where the residual sacrificial layer pattern is removed and conducting the punch-stop ion implantation between the second spacers. Wu **teaches** a method for forming ultra-short channel transistors, wherein the method allows the formation of a gate width narrower than lithographic limitations (Col. 5, lines 55-62). Wu disclose the method comprises forming spacers 20 within a recess portion having an

oxide 12 formed therein (Fig. 3); conducting an ion implantation between the spacers 20 to form a punch-stop ion implant layer 24 (Fig. 3 and Col. 5, lines 63-65); etching the oxide 12 and forming a gate insulation layer 28 (Figs. 4-5 and Col. 6, lines 6-16); and forming a gate 30 (Fig. 6). Wu discloses (in col. 1, lines 15-60) background information explaining why ultra-short channel transistors are an important aspect of high-speed ULSI circuits. Accordingly, it would have been obvious to one of ordinary skill in the art to modify Woerlee by incorporating spacers and punch-stop implantation, as taught by Wu, because such a modification would provide an ultra-short channel transistor.

Regarding claims 2-4 and 7:

Woerlee discloses the first oxide layer 7 is used as an etch stop layer when etching the sacrificial layer to form the residual sacrificial layer pattern 10 (see Fig. 1); the gate insulation layer 24 (Fig. 7) and the gate 21 (Fig. 11) are formed after the source/drain regions 14/15 are previously formed (Fig. 2); the sacrificial layer is formed of polysilicon 8 (Fig. 1); and using the first oxide layer as buffer layer when ion implanting the LDD 11 and the source/drain 14/15 (Figs. 1-2).

Regarding claim 5:

Woerlee (in view of Wu) discloses the claimed invention except for the second oxide being multi-layered. However, applicant has not disclosed that a multi-layered oxide is for any particular purpose or solves any stated problem (note specification, page 6, lines 12-15), and it appears that the invention would perform equally well with a "single" oxide layer (as disclosed by Woerlee). In other words, if so desired, one could modify Woerlee by replacing the second oxide layer with multi-layers of oxides, oxides-and-nitrides, oxide-nitride-oxides, etc., however,

no significant improvement in the manufacturing process (or device performance) would be apparent, but rather, it would seem that processing time would be needlessly increased; therefore, the claim is held obvious over the cited references, especially since one of ordinary skill in the art could obviously choose to incorporate numerous "time consuming" process steps that serve no particular purpose (if so desired).

6. Claims 1, 6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Woerlee** (6,406,963 B2) in view of Yu et al. (6,180,468 B1; hereinafter, "**Yu**").

Regarding claims 1 and 6:

Woerlee discloses all limitations in these claims (see above, in section "5", *Regarding claim 1*) **except** for forming second spacers on side walls of a portion where the residual sacrificial layer pattern is removed and conducting the punch-stop ion implantation between the second spacers, wherein the punch-stop ion implant layer is adapted as a threshold-voltage adjustment ion implant layer. Yu **teaches** a method that provides an ultra-low thermal budget process for channel implant (note Col. 2, lines 17-31), the method comprising the steps of: removing a residual sacrificial layer pattern 24 (Figs. 2-3); forming second spacers 32/34 where the residual pattern 24 is removed (Fig. 4); and conducting an ion implantation adapted as a threshold-voltage adjustment ion-implant layer (Figs. 4-5). Yu discloses the criticality of reducing process thermal budget (note Col. 1, line 48 to Col. 2, line 14); accordingly, it would have been obvious to one of ordinary skill in the art to modify Woerlee by incorporating the process steps taught by Yu because the modification would allow a significant reduction in

process thermal budget, thereby allowing the acquisition of a sharp transition in the doping profile within the channel region (note Yu, paragraph bridging Cols. 1-2).

Regarding claims 8 and 9:

Yu discloses first spacers 26/28 and second spacers 32/34 being formed of nitride layers (Fig. 4 and Col. 3, lines 15-16 and 34-39). Therefore, these claims are held obvious over the cited references.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references listed on the attached Form PTO-892 (not specifically cited above) are cited to show methods for forming short-channel transistors using process steps similar to those of the current invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon-Fri (8 hours each day between 5:30AM and 8:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

CARIDAD EVERHART
PRIMARY EXAMINER

August 26, 2004